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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,982	06/24/2003	Jeff Nause	046361/265061	2036

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ALSTON & BIRD LLP
BANK OF AMERICA PLAZA
101 SOUTH TRYON STREET, SUITE 4000
CHARLOTTE, NC 28280-4000

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,982	NAUSE ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-15 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-15 and 17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/18/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 thru 9, 12, 13, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chavarkar et al. US 2002/0167023 A1 in view of Wolter 4,677,457 in view of Murota et al. US 2002/0109135 A1. Chavarkar discloses (see, for example, FIG. 1) a high electron mobility transistor 10 comprising a two-dimensional electron gas (channel layer) 18, gate contact (gate electrode) 16, and $Al_xGa_{1-x}N$ layer (gate insulating layer) 13. Chavarkar does not disclose a channel layer being composed of a II-VI compound semiconductor zinc oxide. However, Wolter discloses (see, for example, FIG. 3a) a high electron mobility transistor comprising charge carrying layers (channel) 1, 2A, 2B. In column 5, lines 16-26, Wolter discloses the layers comprising gallium arsenide (GaAs) and gallium aluminum arsenide (GaAlAs), however, in

column 7, lines 62-column 8, lines 2, Wolter discloses that GaAs and AlGaAs can be replaced by other semiconductor materials such as ZnO (zinc oxide) in order to utilize different band gaps. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a channel layer being composed of a II-VI compound semiconductor zinc oxide in order to utilize different band gaps in a high electron mobility transistor, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Chavarkar in view of Wolter does not disclose said gate insulating layer having side walls, said gate contact positioned between the sidewalls of said gate insulating layer so that sides of said gate contact face the side walls of said gate insulating layer. However, Murota discloses (see, for example, FIG. 1) a transistor comprising a gate electrode 6, and an insulation layer (gate insulating layer) 7. The gate electrode is bounded by side walls of the insulation layer. It would have been obvious to one of ordinary skill in the art at the time of invention to have said gate contact being bounded by side walls of said gate insulating layer in order to enclose the gate electrode and prevent it from dispersing into the underlying channel layer and prevent any short circuits between source and drain contacts.

Regarding claims 2, 3, 7, and 13, the limitations contain product-by-process language (i.e. epitaxially grown, piezoelectric doping, MOCVD, dummy gate), which does not patentably distinguish the product claims from the prior art.

Regarding claim 4, see, for example, paragraph [0010] wherein Chavarkar discloses $x=0.1\text{-}0.5$ for the $Al_xGa_{1-x}N$ layer.

Regarding claim 5, see, for example, FIG. 1 wherein Chavarkar discloses a substrate 12. FIG. 1 of Chavarkar does not disclose the substrate being at least one of zinc oxide, silicon carbide, sapphire, and silicon and having a bulk resistivity higher than 10^5 ohm-centimeter. However, Chavarkar discloses (see, for example, paragraph [0024]) in another embodiment a substrate made of silicon carbide, sapphire, and silicon. In paragraph [0025], Chavarkar discloses a substrate made of silicon carbide provides the capacity for device isolation and reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the substrate being at least one of zinc oxide, silicon carbide, sapphire, and silicon and having a bulk resistivity higher than 10^5 ohm-centimeter in order to provide the capacity for device isolation and reduced parasitic capacitance.

Regarding claim 6, Chavarkar in view of Wolter in view of Murota does not disclose the thickness of said gate insulating layer ranging from 0.30 nanometer (nm) to 50 nm. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the thickness of a gate insulating layer in order to provide insulation between the gate and channel layer so that a current is formed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the thickness of said gate insulating layer ranging from 0.30 nanometer (nm) to 50 nm because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the thickness of a gate insulating layer in order to provide insulation between the gate and channel layer so that a current is formed. See In re Aller, 105 USPQ 233.

Regarding claims 8, and 9, see, for example, FIG. 1 wherein Chavarkar discloses a gate contact 16, and source/drain contacts 15,17. FIG. 1 of Chavarkar does not disclose the gate

contact being selected from the group consisting of titanium, platinum, silver, gold, chromium, alloys of titanium and tungsten, and platinum silicide, and the source and drain contacts comprise an alloy of titanium, silicon, aluminum, and nickel. However, Chavarkar discloses (see, for example, paragraph [0031]) in another embodiment a gate contact made of titanium, platinum, chromium, alloys of titanium and tungsten, and platinum silicide, and source/drain contacts made of alloys of titanium, aluminum, or nickel. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate contact being selected from the group consisting of titanium, platinum, silver, gold, chromium, alloys of titanium and tungsten, and platinum silicide, and the source and drain contacts comprise an alloy of titanium, silicon, aluminum, and nickel in order to provide electrical contacts of adequate conductivity.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chavarkar et al. US 2002/0167023 A1 in view of Wolter '457 in view of Murota et al. US 2002/0109135 A1 as applied to claims 1-9, 12, 13, and 17 above, and further in view of Shanfield et al. 5,880,483. Chavarkar in view of Wolter in view of Murota does not disclose a passivation layer on said gate contact and said source and drain contacts. However, Shanfield discloses (see, for example, Fig. 3) a field effect transistor comprising a passivation layer 36 over a gate electrode 24, source electrode 20 and drain electrode 22. The passivation layer protects the top of the field effect transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a passivation layer on said gate contact and said source and drain contacts in order to protect the top of the transistor.

6. Claims 14, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chavarkar et al. US 2002/0167023 A1 in view of Wolter '457 in view of Murota et al. US 2002/0109135 A1 as applied to claims 1-9, 12, 13, and 17 above, and further in view of Nishikawa et al. 6,323,053 B1. Chavarkar in view of Wolter in view of Murota does not disclose a ZnO substrate and the ZnO substrate being a c-surface substrate. However, Nishikawa discloses (see, for example, column 11, lines 50-55) a semiconductor device comprising a substrate made of ZnO and further discloses that a C surface can be used. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a ZnO substrate and the ZnO substrate being a c-surface substrate in order to have a stable base to form a semiconductor device thereon, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chavarkar et al. US 2002/0167023 A1 in view of Wolter '457 in view of Murota et al. US 2002/0109135 A1 as applied to claims 1-9, 12, 13, and 17 above, and further in view of Ando 6,429,467 B1. Chavarkar in view of Wolter in view of Murota does not disclose the gate insulating layer being formed by metal organic chemical vapor deposition (MOCVD). However, Ando discloses (see, for example, column 4, lines 43-60) a field effect transistor comprising a gate insulating layer 13 wherein the gate insulating layer is formed by MOCVD. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate insulating film being

formed by metal organic chemical vapor deposition (MOCVD) in order to adequately form the gate insulating film in a transistor.

Response to Arguments

8. Applicant's arguments with respect to claims 1-10, 12-15, and 17-19 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
August 29, 2005